The Structure and Electrical Properties of Porous Silicon Prepared by Electrochemical Etching

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Abstract

Porous silicon was prepared by using electrochemical etching process. The structure, electrical, and photoelectrical properties had been performed. Scanning Electron Microscope (SEM) observations of porous silicon layers were obtained before and after rapid thermal oxidation process. The rapid thermal oxidation process did not modify the morphology of porous layers. The unique observation was the pore size decreased after oxidation; pore number and shape were conserved. The wall size which separated between pore was increased after oxidation and that effected on charge transport mechanism of PS.

Key words

Electrochemical etching,

Porous silicon, SEM images

Article info

Received: Sep. 2010
Accepted: May. 2011
Published: Oct. 2011

الخصائص التركيبية و الكهربائية للسليكون المسامي المحضر بطريقة القشط الكهروكيميائي

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الخلاصة

في هذا العمل ، تم تحضير السليكون المسامي باستخدام طريقة القشط الكهروكيميائي. الخصائص التركيبية،الكهربائية والخصائص الكهروضوئية تم انجازها. ملاحظات المجهر الالكتروني الماسح لطبقة السليكون المسامي تم الحصول عليها قبل وبعد عملية الأكسدة الحرارية السريعة. عملية الأكسدة الحرارية السريعة لاتحور طبوغرافية طبقة السليكون المسامي . الملاحظة الوحيدة كانت حجم المسام يقل بعد عملية الأكسدة. بالإضافة إلى ذلك ،كثافة المسام بقية محفوظة. حجم الجدار الذي يفصل بين المسام ازداد بعد عملية الأكسدة وهذا اثر على ميكانيكية انتقال الشحنة للسليكون المسامي .

Introduction

Porous silicon (PS) becoming an increasing important and versatile electronic material in today's fabrication technology .Its reactive porous nature allows for the selective formation of unique electronic components and mechanical nanostructures [1]. The low temperature oxidation of porous silicon and the electrochemical conversion of porous silicon to oxide have already been utilized in electronic isolation technology although commercial devices are yet to come [2].

For p-type Si, the holes are the majority charge carriers, so the p-type PS (p-PS) layers are easily produced. Conversely, n-type PS (n-PS) is very difficult to form, because of the lack of holes. Previously, most of the research done on PS has been made on hole-rich p-type Si. Up until now, to get an n-PS layer, illumination has still been the popular way (even indispensable way) to

generate the holes required in the electrochemical etching process on the hole-poor n-type samples [3].

The electrical properties and conduction mechanisms is important, differences in structural characteristics of PS and in the multifunction properties of PS based nano structures give rise to the observed diversity of electrical properties. The optoelectronic applications such as light-emitting devices, photo detectors and solar cells and sensing devices using PS active layer require proper understanding of electronic transport behavior of PS layers in device structures, especially the junction properties. The transport of carriers within the PS layer thickness and across the *c*-Si/PS heterojunction governs the device characteristics [4-6]. Some of research considers PS is isotype hetrojunction since it is reported to be n-type when it is fabricated from n-type substrates [6, 7].

Pulsford et al. [8] reported that the porous silicon behaves like n-type when it is formed on a p-type silicon substrate because of the depletion process in the porous layer. The depth of depletion region depends on carrier concentration, and extends to a distance of few tenths of microns into silicon, taking into account that silicon rods in porous silicon film have a thickness in the range of nanometer, which is at least two orders less than the depletion width, it can easily be inferred that the bulk of porous silicon is depleted of electrons. Depleted porous silicon forms an ohmic contact with the aluminum top electrode. Reverse current exhibits soft breakdown voltage. This behavior is an indicative of the carrier transport through hetero structure [9].

The three most common mechanisms have been proposed to explain the rectifying properties of PS diodes ; (i) supply of minority carriers from the Si substrate or barrier at the PS/Si junction, (ii)Schottcky barrier at the $contact_1$/PS/ junction and (iii)p-n junction within PS layer for PS made from a c-Si p-n junction[4].

In this work, is proposed to use porous silicon layer as optoelectronic device and studying the rapid thermal oxidation effect on structure, electrical, and photoelectrical properties. The scanning electron microscopy (SEM) type JSM-5510 with a resolution down to (10 nm).The given voltage for each image was (20 KV).

Experimental

Electrochemical etching of p-Si wafers in electrolytes including hydrofluoric acid (HF) and surfactants (mainly ethanol) forms the PS structure. Ethanol is often added to facilitate evacuation of H_2 bubbles; these bubbles can easily leave the surface because of the decreased surface tension of the liquid. To be able to synthesize uniform layers with high reproducibility, the applied anodic current density and etching time are monitored, controlled and kept at a particular constant level required during the process [4]. Typical anodization arrangements are schematically shown in Fig.1.

In this work, the porous silicon was prepared from single crystalline p-type silicon (100) oriented and resistivity (7-10)Ω.cm with thickness 508 μm. The electrical circuit of electrochemical etching could be shown in fig.1; it is completely after putting a Pt electrode in parallel way to achieve the homogenous PS layers. Current density of about(50 mA/cm^2) applied for etching time (10 min).The rapid thermal oxidation (RTO)system is consisted from the following :(1) a tungsten halogen photo optic lamp type (OSRAM 64575) with power 1000 W based on ceramic base. A parabolic reflector like half circuit was put under the lamp to increase the heating efficiency. (2)A quartz tube have

2 cm diameter opening from two sides to circulate the dry oxygen source. The quartz tube attached with halogen lamp to obtain the must-wanted temperature.

The various RTO temperatures ranged (773-973) K at oxidation time 60 sec can be measured by calibration using thermocouple with a digital reader, which has been located above the sample.

The photoelectrical properties were done by employing it was obtained by using varic type (TDGC2 –KVA voltage regulator) connected with a lamp to obtain on most wanted intensity.

Results and Discussions

Fig.2 shows SEM micrographs for the surface of PS prepared by electrochemical etching at current density 50 mA/cm^2 and etching time 10 min before and after oxidation process, where. The pore size was measured directly from these micrographs.

It could be seen that the pore network (in black) separated by silicon crystallites (in white).For sample (a), pore size varied from (0.004 to 0.02μm), while for sample (b) the pore size was varied from (0.005 to 0.05 μm), this meaning that after oxidation the pore size will be decreased due to growth oxide inter pore this result consisted with *Pirasteh et al* observation [10]. By comparing Fig.2 a and b, our can see that after oxidation, the pore shape is conserved in spite of size reduction.

Moreover, the wall size that separate pores can be evaluated from these micrographs. That increase due to the volume expansion of silicon transformed into oxidized silicon. However, the pores did not collapse because of the initial porosity which was more important than volume expansion and the structure was allows open on the surface. Therefore, the density was nearly the same before and after oxidation and it were about 3×10^4 pore /cm^2 this result consisted with *Charrier et al* observations [11].

The porous layer thickness measured by employing high resolution optical microscope (OLUPUS BH2) type with resolution down to 600X ,the optical microscopy connected with computer and digital camera, the porous layer thickness was (10-18) μm this difference in thickness due to some of pore etched greater than others, we take the average of these value ,the porous layer thickness was 14 μm.

The D.C measurements were made in dark for a number of PS/Si and PS/ OPS/ Si samples .The deviations of I-V characteristics for thick PS layer from the ideal one is due to the existence of series resistance (Rs). Forward I-V dependence therefore is analogous to that of diode with series switched resistance [4]:

$$J = Js\left[\exp\frac{q(V-IR_s)}{mkT}-1\right] \quad .....(1)$$

where Js is the saturation current obtained from semi-log forwarded bias, k is Boltzmann constant(1.38×10^{-34}J/K), T is absolute temperature in Kelvin and q is electron charge (1.6×10^{-19}C).Series resistance R_s is voltage dependent ,it is also depends on the thickness and porosity of the PS layer [4], therefore the determination of saturation current value from extrapolating the measured forward bias IV curve is not quite credit prove and shows difficulties to determine by several works. We therefore measured the saturation current directly under forward bias conditions beside the extrapolating saturation current at zero bias to assure the validity of results. The measurements of the saturation current under forward bias voltages for PS before and after rapid thermal oxidation (RTO) treatment and plotted in semi-log graphs as shown in Fig.3.

Fig.3, shows that the decreasing of saturation current density after oxidation process because of the presence of oxide layer working to decrease transmission of minority carrier from semiconductor to metal so the rectification ratio will be increased, where the rectification ratio increased from (3.9 to 57.5) as shown in Table.1.Also one can observed that the barrier height which is governed by thermonic emission equation [4]:

$$J_S = A^{**}T^2 \exp\left(-q\Phi_{Bn}/KT\right).....(2)$$

The barrier height (Φ_{Bn}) can be calculated using the following equation [12]:

$$\Phi_{Bp} = \frac{KT}{q} Ln \frac{A^{**}T^2}{J_S}.....(3)$$

where A^{**} is the effective Richardson's constant, which equals 32($A/K^2.cm^2$) for p-type silicon and Φ_{Bp} (eV) is the barrier height could be shown in Table1.It is observed that increasing barrier height after oxidation process , where it varied from (0.56 to 0.69) eV,is attributed to the oxide thickness affected on the transport mechanism and manufacture to difference in Fermi level, we get to the additional limit in barrier height equation due to oxidation which can be seen in this equation [12]:

$$\phi_T = \frac{kT}{q} Ln \frac{A^* T^2}{J_S} + \frac{kT}{q}\chi^{1/2}\delta.....(4)$$

The equation (4) can be written as the following [12]:

$$\phi_T = \phi_{Bp} + \frac{kT}{q}\chi^{1/2}\delta.....(5)$$

where χ is the average barrier height due to oxide layer (eV), δ is the oxide thickness (Å) which given inTable1.The oxide layer thickness calculated theoretically from the following relationship [13]:

$$R_0 = 1.8\times10^5 \times e^{-1.21eV/KT}.....(6)$$

where R_0 is the average initial RTO growth rate in Å/s and 1.21 eV represent activation energy [13].

The dark current which shown in Table 1. is observed increased with increasing oxidation temperature, it could be due to the defects formed by non-stoichiometric silicon –oxide and they would act as tunneling centers [14], the dark current at oxidation temperature 973 K was decreased because the oxide layer is thicker at oxidation temperature 973 K and the tunneling probability of thermally generated carriers through the oxide layer are reduced and hence the dark current are reduced this result consisted with *Mehrdad et al* and *Stevenet* observations [13, 14].

The photocurrent of PS before and after RTO process at reverse bias 5V under illumination power density 200 mW/cm^2 given in Table 1.The photocurrent is decreased at oxidation temperature 773 K and 873 that because the oxide thickness is low at lower oxidation temperature which it plays as a defect in device leading to increase saturation current as a result to increase dark current that lead to decrease photo current [14].After that the photocurrent will be increased about 13 times rather than fresh PS sample at oxidation temperature 973K this is due to many reasons:1) Increase in barrier height caused to increase built in potential ,which is lead to increase the depletion layer width according to relation[4]:

$$W = \sqrt{\frac{2\varepsilon V_{bi}}{qN_e}}.....(7)$$

where W is the width of the depletion layer and V_{bi} (V) is the built in voltage is determined by the intercept at $1/C^2=0$ by extrapolating the curve to the voltage axis, and N_d (cm^{-3}) is the density of

carrier in the porous layer and it equal to the following equation[4] :

$$N_e = \frac{2}{q\varepsilon_{si}\zeta^2}\frac{dV}{dC^{-2}} ......(8)$$

where ε_{si} is the silicon permittivity, dV/dC^{-2} is the slope reciprocal, and ζ is the factor depending on the carrier concentration of silicon substrate, which is equal to 0.2 for P-type silicon [4].The increasing in the depletion layer width lead to increase photocurrent according *Timokhov et al* [15], which the photocurrent in Al/PS/c-Si/Al sandwich structures is related to the incident light flux (Φ) by the expression [15]:

$$I_{Ph} = q\phi Q = \mathrm{q}\phi\gamma\beta\alpha .....(9)$$

where q is the electronic charge , *Q* is the quantum photosensitivity of PS/c-Si hetrojunction,γ is the factor shown which portion of the light flux will be absorbed in PS/c-Si hetrojunction , β is the quantum output of an internal photo effect ;α is the factor of division of PS/p-Si hetrojunction (ϕ being photon flow, quantum/cm^2 sec).The factor γ, with the accounting of repeated internal reflection has the following dependence from κ, ι and factor of reflection R:

$$\gamma = \frac{(1-R)(1-e^{-\kappa\iota})}{1-\mathrm{Re}^{-\kappa\iota}} .....(10)$$

From this follows that at κ < ι factor γ~ κ and smoothly grows at the further increase of κ, aspiring to the limiting value γ=1-R.Therefore ,the diagram of γ versus *hv* will also like an increasing curve striving for limiting value 1-R,which is achieved at *hv* < Eg, κ =W^{-1} and L_n^{-1},L_p^{-1}>> ι^{-1}.So:

$$\alpha = \frac{W + L_n + L_p}{d_{ps}} .....(11)$$

where W is the width of the depletion layer, d_{ps} is the thickness of the porous layer, L_n and L_p are the diffusion lengths of minority carriers. The total photocurrent is given by [15]:

$$I_{Ph} = q\phi\gamma\beta\frac{W + L_n + L_p}{d_{PS}} .....(12)$$

From this equation we can observed that the photocurrent is proportion to the width of the depletion layer. In this work, the photo current was measured from the relation[12]:

$$I_{Ph} = I_b - I_d .....(13)$$

where I_b represent current under illumination, and I_d represent current in dark under reverse bias.

(2) The second reason to interpret the increasing of photo current with increasing oxidation temperature due to the oxide layer caused to decrease the interface state at the contact region PS/ c-Si subsequently decrease the recombination process that increasing the number of carrier which reach to the depletion layer[14] .Otherwise the oxidation leads to decrease minority –carrier recombination velocity in the interface junction between PS/Si to insure the relation [16]:

$$\frac{S_0 L}{D} << 1.....(14)$$

where S_o is the surface recombination velocity, L and D are the diffusion length and the diffusion coefficient of the minority carriers ,the diffusion length could be measured by capacity-Photocurrent measurements, *Timokhov et al*[15] found that the minority charge length for various samples PS laid in limits from 0.15 to 0.65 microns.

In respectably the conventional photo diodes the main parts of the radiation from this range are lost because of strong absorption and the resultant recombination of photo carriers on the

illumination surface and in the surface layer, giving rise to a short time. After oxidation, the incident radiation passes through a SiO_2 film which acts both as a protective and antireflection coating, and this radiation generates electron-hole pairs directly in the photo diode base [16].

Fig.4 shows the photo current under different illumination power and reverse bias 5V. One can observe that increasing of photo current with increasing illumination power density that due the generation rate of electron hole pairs (G) proportion with illumination power per unit time that consisted with researches observation [17-19] according to the following equations [17]:

$$G = \eta N_p .....(15)$$

where G is the density of electron hole pairs generated per unit time, η is the quantum coefficient of Si ,typically 0.85 at incident light has wavelength 780 nm, N_p is the number of photons irradiated on silicon wafer per unit time and it given by the following equation [17]:

$$N_P = \frac{P}{hv} .....(16)$$

where P (W)is the power of light, hv (eV)is the energy of photon, and v(HZ) is the frequency of incident light. The N_p could be measured by photo counter rate which count the number of photon in per second.

way to obtain lower optical loss of PS optoelectronic device by reducing volume scattering and reflection also the oxide layer acts both as a protective and antireflection coating.

Acknowledgment:

The author would like to acknowledge, University Sian Malaysia (USM). (SEM) measurements were carried out in the School of Physics / Nanostructures and Optoelectronics Research Center (NOR)-lab /University Sian Malaysia

Conclusions

Porous silicon was prepared by using electrochemical etching process. The structure, electrical, and photoelectrical properties have been performed. Scanning electron microscopic observations obtained before and after rapid thermal oxidation process on porous silicon**.** The electrical properties under our optimum preparation conditions; rectification ratio was increased from 3.9 to 158.8, barrier height was changed from 0.56 to 0.69eV,dark current was decreased from 541 to 317 $\mu A/cm^2$ photocurrent was increased from 1956 to 25873$\mu A/cm^2$ (under 200 mA/cm^2 tungsten lamp illumination) .That meaning the oxidation process of PS layers is a good.

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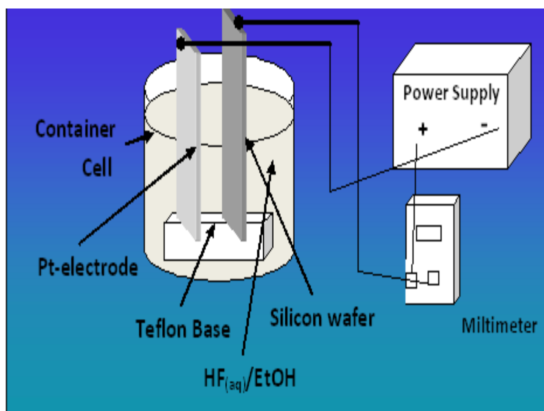

Fig.1:Schematic digram depicts the electrochemical etching system.

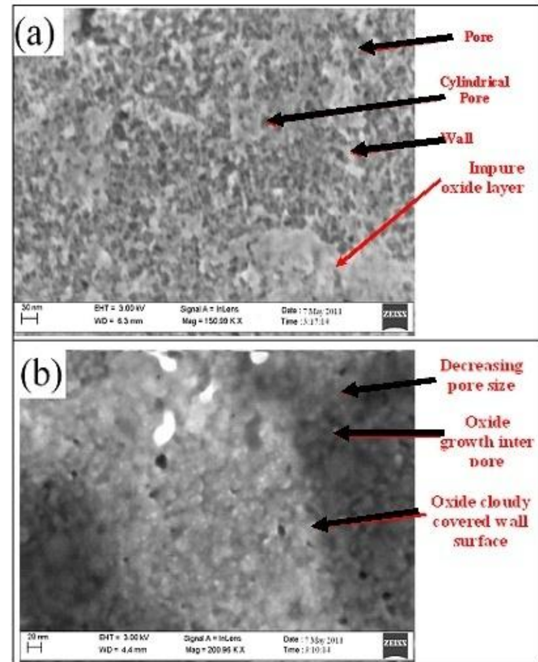

Fig.(2):PSEM image of PS (a) without oxidation, (b) at oxidation temperature 973K and 60 sec

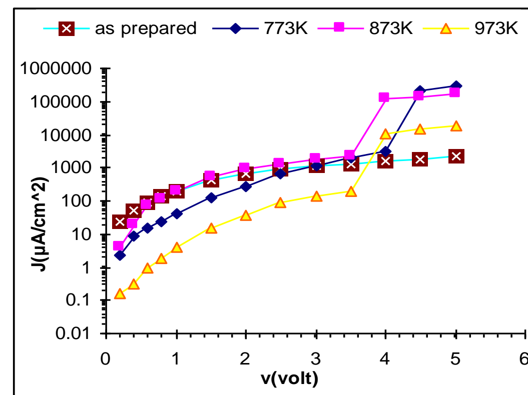

Fig.3: Saturation current density of PS before and after RTO process.

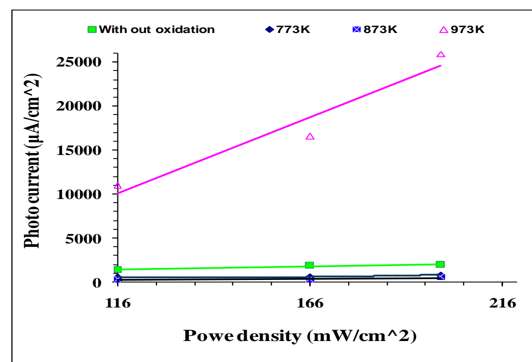

Fig.4: Shows photocurrent of a PS photo detector before and after RTO process at reverse voltage (5volt) for different illumination power density.

Table 1.Shows the electrical characteristics of PS before and after RTO process

Temperatures (K)	Oxide thickness (nm)	Rectification ratio	Barrier height (eV)	Dark current (μA/cm^2)	Photocurrent density (μA/cm^2)
0	0	3,93	0,56	541,25	1956,25
773	0.014175	158,8	0,63	1800	800
873	0.113337	39,5	0,62	4166,667	555,556
973	0.591078	57,5	0,69	317,4603	25873